REMARKS

Claims 1 through 24 are currently pending in the application.

Claims 12-24 have been withdrawn from consideration.

Claims 1 through 11 stand rejected.

This amendment is in response to the Office Action of October 7, 2002.

Drawings

Applicant submits herewith, under cover of a separate Letter to the Chief Draftsman, for proposed correction to drawing FIG.7 of the drawings. All proposed corrections have been marked in red. Applicant respectfully requests approval of the corrections to the drawings and will file corrected formal drawings upon receipt of such approval in the application. Applicant submits that the drawing correction clearly complies with 35 U.S.C. § 132 as no new matter has been introduced into the application. Applicant submits that the correction to drawing FIG. 7 and the description thereof in number paragraph **[0058]** is supported by drawing FIG. 9 and the description thereof in paragraph numbered **[0060]** of the specification.

35 U.S.C. § 112 Claim Rejection

Claims 1 through 11 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention.

Applicants have amended the claimed invention for the presently claimed invention to particularly point out and distinctly claim the subject matter of the invention to comply with the provisions of 35 U.S.C. § 112. Therefore, presently amended claims 1 through 11 are allowable under the provisions of 35 U.S.C. § 112.

35 U.S.C. § 101 Double Patenting Rejection

Claims 1 through 11 stand rejected under 35 U.S.C. § 101 as claiming the same invention as that of claim 2 of prior United States Patent 6,337,227 (hereinafter referred to as the `227

patent. Applicant respectfully traverses this rejection, as hereinafter set forth.

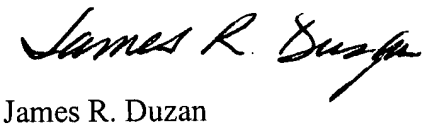
Applicant submits that a reliable test for double patenting under 35 U.S.C. § 101 is whether a claim in the application could be literally infringed without literally infringing a corresponding claim in the patent. Is there an embodiment of the invention that falls within the scope of one claim, but not the other? If there is such an embodiment, then identical subject matter is not defined by both claims and statutory double patenting would not exist. *In re Vogel,* 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

Applicant submits that the `227 patent requires as an element of the embodiment of the claimed invention "aligning vertically said first semiconductor substrate element and the at least one second semiconductor substrate element to vertically align integrated circuitry on said first semiconductor substrate element and at least one of the plurality of integrated circuits on said at least one second semiconductor substrate element' whereas the presently claimed invention of amended independent claim 1of the present application contains no such element of the invention thereby, clearly, claiming a different embodiment of the invention. Accordingly, Applicant submits that no double patenting under 35 U.S.C. § 101 exists between presently amended independent claim 1 of the present application and any embodiment of the inventions claimed in the `227 patent. Therefore, claims 1 through 11 are allowable.

Applicants submit that claims 1 through 11 are clearly allowable over the cited prior art.

Applicants request the allowance of claims 1 through 11 and the case passed for issue.

Respectfully submitted,



James R. Duzan
Registration No. 28,393
Attorney for Applicant
TRASKBRITT
P.O. Box 2550
Salt Lake City, Utah 84110-2550
Telephone: 801-532-1922

Date: January 7, 2003
JRD/jml:djp

Enclosure: Version with Markings to Show Changes Made

Document in ProLaw

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

A marked-up version of paragraph **[0001]**, highlighting the changes thereto, follows:

[0001] This application is a continuation of application Serial No. 09/651,394, filed August 29, 2000, [pending] now U.S. Patent 6,337,227 B1, issued January 8, 2002, which is a continuation of U.S. Patent Application Serial No. 08/844,669 filed April 18, 1997, now U.S. Patent 6,165,815, issued December 26, 2000, which is a continuation of U.S. Patent Application Serial No. 08/650,429, filed May 20, 1996, abandoned.

A marked-up version of paragraph **[0058]**, highlighting the changes thereto, follows:

[0058] FIG. 7 illustrates a side plan view of alternative die assembly 700 of the present invention. FIG. 7 shows a TAB attachment assembly rather than the wirebonding shown in FIG. 6. The alternate die assembly 700 is similar in structure to the die assembly 600 of FIG. 6; therefore, components common to both FIG. 6 and FIG. 7 retain the same numeric designation. A plurality of traces 704 on dielectric TAB firms 702 are attached between the upper die bond pads 626 and corresponding trace or lead ends or other terminals 630 on the upper surface 614 of the substrate 606. It may be desirable to employ a heat sink member 912 between the semiconductor substrates 602 and 604, either embedded in the adhesive or located between two adhesive layers, to promote heat transfer from the semiconductor substrates 602 and 604.

IN THE CLAIMS:

A marked-up version of each of the presently amended claims, highlighting the changes thereto, follows:

1. (Twice Amended) A method of fabricating a multi-level stack of semiconductor substrate elements, each semiconductor substrate element of said substrate elements including integrated circuitry, comprising:

providing a first semiconductor substrate element having a first side including integrated circuitry thereon and having a back side;

providing a [at least one] second semiconductor substrate element having a first side including [a plurality of] integrated circuitry thereon and having a backside;

stacking said first semiconductor element and said at least one second semiconductor substrate element in a superimposed relationship having the back side of the first semiconductor substrate element facing the back side of the [at least one] second semiconductor substrate element [aligning vertically], said first semiconductor substrate element and the [at least one] second semiconductor substrate element for locating [to vertically align] a portion of the integrated circuitry on said first semiconductor substrate element adjacent [and] a portion [at least one] of the [plurality of] integrated circuitry [circuits] on the [said at least one] second semiconductor substrate element; and

severing from said stack traversely at least one dice pair comprising a die from said first semiconductor substrate element and a [an aligned] second die from said at least one second semiconductor substrate element; and

adhesively attaching said first semiconductor substrate element and said at least one second semiconductor substrate element.

2. The method of claim 1, wherein said adhesive comprises a dielectric adhesive.

3. The method of claim 1, further including:
disposing a heat sink element between said first semiconductor substrate element and said at least one second semiconductor substrate element.

4. (Twice Amended) The method of claim 1, wherein said first semiconductor substrate element and the [at least one] second semiconductor substrate element, each semiconductor substrate element of the first semiconductor element and the second semiconductor element including locations defining discrete dice or wafer portions severable from a first semiconductor substrate wafer and at least one second substrate wafer.

5. (Previously Amended) The method of claim 1, wherein said first semiconductor substrate element and said at least one second semiconductor substrate element each include a flat, and said vertical alignment is effected by aligning said flat of said first semiconductor substrate element and said flat of the at least one second semiconductor substrate element.

6. (Amended) The method of claim 1, further comprising:
connecting a first die of said at least one dice pair to conductors of a substrate having conductors.

7. The method of claim 6, wherein said connection is selected from a group comprising reflowable metal elements, polymer elements having a conductive capability, and preformed lead-type elements.

8. The method of claim 6, further comprising:
connecting both dice of said at least one dice pair to conductors of said substrate.

9. The method of claim [1] 6, further comprising:
connecting the second die of said at least one dice pair to portions of the conductors of said substrate through intermediate connection elements.

10. (Previously Amended) The method of claim 9, wherein said intermediate connection elements are selected from a group consisting of bond wires and traces of flex circuits.

11. (Twice Amended) The method of claim 10, further comprising:
connecting said at least one dice pair to portions of the conductors of said substrate and
encapsulating said at least one dice pair thereafter.